IC 3A, 7F, 7G: 7474 D Flip Flops:
$C900 Bit 0
$C900 Bit 1
$C900 decoded with 3B + 2C: 2C enables 3B decoder 2 when address Cxxx appears (this indicates I/O control)
3B decoder 2 partially decodes $x9xx with A10=0, A11=1 --> 3B output 2Y2 is low, and enables decoder 1 in 3B
3B decoder 1 partially decodes $x9xx with A8 = 1, A9 = 0 ---> 3B output 1Y1 is low when A8 = 1, A9 = 0, A10 = 0, A11 = 1 ==== $x9xx
"E" / "E*" signal is an external clock input to the 6809 generated by 7K, 7G (4 MHz clock) switching E on and off
"E*" input to 2B to cause clock pulse to 3A on a Write* to $C900, latching Bit 0 / Bit 1 into 3A Set or clear EROM signal to read from ROM or RAM
2D checks for Read with EROM high, causing 3E to go low, enabling 2C ROM chip select outputs "Screen Control" is the signal to flip the display for coctail mode
2D also causes 3E to go low for any memory access with A14 = A15 = 1, to banks C, D, E, F

3E cannot be bad since it enables ROM chip select, and test program reads from ROM, and executes memory test
If memory test is in a ROM bank D, E, or F, then only one of the two AND gates in 2D needs to work (pins 3, 4, 5, 6 or pins 8, 9, 10, 11)
Tried 2 different ROM 0s, but maybe both were bad?
2-0-1 Error: cannot read bank 0 ROM --> 2D gate on pins 8, 9, 10, 11 is bad?
2-0-1 Error: 2C output 0 might be bad
2-0-1 Error: EROM generation might be bad: 3A flip flop, or 2B, or 3B; if so, would not be able to read from any of ROM 0 - 9
2-0-1 Error 3A flip flop was bad; replaced and Stargate boots